Module-20
Shift Registers

1. Introduction
2. Types of shift registers
   2.1 Serial In Serial Out (SISO) register
   2.2 Serial In Parallel Out (SIPO) register
   2.3 Parallel In Parallel Out (PIPO) register
   2.4 Parallel In Serial Out (PISO) register
3. Bidirectional shift register
4. Universal shift register
5. Ring counter
6. Johnson counter
7. Shift register ICs
8. Applications of shift registers
9. Summary

Learning Objectives:

1. To study the data shift/transfer in different registers
2. To understand the construction and working of different shift registers.
3. To learn the sequence of operation of Ring and Johnson counter
4. To know the applications of shift registers.
1. Introduction

In almost all cities, we see various big rolling displays advertising different products or sales. This is one of the most popular applications of shift register. Text/image can enter from left or right and moves out sequentially. Similarly, data can be loaded in parallel from top and leaves towards bottom. For long distance data communication, shift register can convert slow parallel data into high speed serial over single wire and serial to parallel at a receiver end. This helps in reducing the cost of data transmission.

Shift registers like counters are basically some form of sequential circuit. Unlike combinational circuit, sequential circuit outputs are not only dependent of present inputs but also on the past inputs as well.

Flip flops are used for storing binary information. Single flip flop can store 1-bit binary data either 0 or 1. To increase the storage capacity, we need to use group of flip flops. Register is a group of flip flops connected together to store multiple bits. The n-bit register consist of n number of flip flops and is capable of storing n-bit information. For example, 8-bit register can store 8-bit data for a computer and requires 8 flip flops. Binary data can be entered serially or parallel into the register. Similarly, the data can be shifted out in serial or parallel out on every clock pulse.

Shift registers are classified into 4 types depending upon how the data is shifted in and shifted out either serially or parallel. In addition, there are bidirectional shift registers, ring and Johnson counter. There are MSI shift registers available commercially in TTL as well as in CMOS families. Let us now study the shift registers in this module.

2. Types of shift registers

Shift registers are a type of sequential logic circuit. Shift register has two important keywords. The first one is shift and the second is register. Register is basically a group of flip flops connected in such a way that binary number can be entered into the register. Single flip flop can store only 1-bit data. For storing n-bits, n flip flops are required for storage. Shift register is capable of storage as well as shift or data transfer.

For handling the binary data, there are two main operations Shift-In for data entry and Shift-Out for data transfer or exit. Both the operations can be implemented either bit by bit i.e. serially or all-bits-simultaneously i.e. in parallel.
Shift registers can have serial or parallel inputs and outputs. There are some shift registers that have both serial and parallel inputs and outputs as shown in figure 1.

Classification of shift register depends on how the data is shifted IN and shifted-OUT i.e. whether the data input and output are serial or parallel. There are four basic types of shift registers:
1. Serial In Serial Out (SISO) shift register
2. Serial In Parallel Out (SIPO) shift register
3. Parallel In Serial Out (PISO) shift register
4. Parallel In Parallel Out (PIPO) shift register

When the data is to be moved serially both at the input or output, the type of shift register used is serial in serial out (SISO).

If the data is fed serially at the input and is retrieved in parallel manner at the output, the shift register is known as serial in parallel out (PISO). This action results in serial to parallel conversion.

When data is entered in parallel and taken out in a serial fashion, the shift register is called parallel in serial out (PISO) register. This shift register is also called parallel to serial converter. Finally, if both the input and output are in parallel manner, the shift register is termed as parallel in parallel out (PIPO) register.

In all four types, the storage as well as transfer of data takes place only upon the applications of clock pulses. When the clock is absent, the original data is retained till power is on and shift register acts like a temporary memory.
The possible ways of data movements in a shift register are shown in figure 2. Registers are implemented using flip flops that provide storage capacity. In this case, a 4-bit shift register is used for shift and storage. The arrow indicates the direction and type of data transfer. Data is entered serially and shifted right or left. It is also possible to introduce rotate right or left operation using closed loop path. Serial operation requires at least four clock pulses for 4-bit register to shift the data to left or right. For faster operation, data can be entered in using parallel shift in operation or parallel shift out in single clock cycle.

Figure 3: SR, D and JK flip flops as basic elements of shift register
Shift registers can be constructed using simple SR, D or JK flip flops. Figure 3 indicates the FFs as the basic elements of shift register. Flip flops can be either positive or negative edge triggered flip flop. In case of counter, JK flip flops are usually used in toggle mode of operation. Whereas in a shift register, it is possible to use SR, JK or D flip flop in set, reset or hold mode. Single flip flop acts as a 1-bit storage register. With the proper interconnections of the flip flops it is possible to decide the type and storage capacity of the shift register. In the next section, let us discuss the construction and working of different types of shift registers.
2.1 Serial In Serial Out (SISO) shift register

The serial in serial out (SISO) shift register is a simply collection of clocked flip flops linearly connected. This register accepts data serially (one bit at a time) and shifts or moves the data serially through various stages of the registers and exits form last flip flop serially.

![Serial In Serial Out shift register diagram](image)

Let us consider a 4 bit shift register constructed using four D-flip flop in cascade as shown in figure 4. External serial data is fed to the first D flip flop and data exits serially from the fourth i.e. last flip flop. Each flip flop has its outputs connected to the inputs of the next in line. The same clock input goes to all flip flops and they are all negative edge triggered.

Let us study the operation of SISO register. The shift register is initially in clear state i.e. (Q0 Q1 Q2 Q3= 0000). Consider data to be entered as 0101. Data must be entered beginning with right most bit first (LSB). The serial data input ‘1’ is applied to the first FF. When the first clock pulse is applied, the first FF output becomes Q0=1. The register contains now 1000. Now the second bit is applied to the data input. D=0 for first flip flop and D=1 for the second flip flop. When second clock pulse is applied, at negative transition, The second FF output Q1 changes to 1 and Q0 becomes 0. The register contains now 0100. The third bit 1 at serial input is allowed to store in the first FF with the third clock pulse. The 0 stored in first FF is shifted to second flip flop and 1 stored in second flip flop is shifted to third flip flop. The register output is 1010. With the fourth clock pulse, the last bit 0 is present at serial input and is shifted into first flip flop and Q0 becomes 0. Bit stored in first FF is shifted to second FF i.e. 1. The 0 stored in second FF is shifted to third FF. The LSB =1 stored in third FF is shifted to last FF. The register now contains 0101.

After shift in operation, first (right most) bit of serial data is available at the serial data output. The second data bit is shifted out at the next clock transition. Similarly third bit is also shifted out and last bit is available with next clock transition The register is of right shift type and the stored data is shifted out of the right and lost after eight clock cycles.

Let us summarize the operation. In SISO register, first bit is entered into the register on the first clock pulse and then shifted from left to right as remaining bits are entered and shifted. In such register, for serial data one bit at a time is transferred into or out of the register. Therefore, 4 clock pulses are required to transfer the data into the register and additional 3 clock pulses are required to shift data out of the register serially.
2.2 Serial In Parallel Out (SIPO) shift register

For a 4-bit SIPO shift register, there is one data input, 4-outputs and one clock input as shown in figure 5. In such register the data is enter serially just similar to SISO shift register. First bit is entered into the register on the first clock pulse and then shifted from left to right as remaining bits are entered and shifted. In such register, for serial data one bit at a time is transferred into the register. Therefore, 4 clock pulses are required to transfer the data into the register.

There is difference in a way the data bits are shifted out of the register. Once the data are stored in the register, each bit appears on respective output lines of flip flops. As all bits are available simultaneously, the shift register provides parallel out lines.

2.2 Parallel In Serial Out (PISO) shift register

This type of shift register accepts data in parallel form and outputs it in serial form. With a single clock pulse, data bits are entered simultaneously into the respective flip flop stages of the shift register and output is available bit by bit from last storage. For PISO register, it is necessary to shift the data after loading it in parallel. But unfortunately, the two acts - parallel loading and shifting serially cannot occur simultaneously. This is achieved using AND-OR logic as shown in figure 6.

![Figure 5: Serial In Parallel Out shift register](image)

![Figure 6: Combinational block for PISO shift register](image)
There are two AND gates. One of them receives parallel data bit and the other receives output of previous FF for shifting. The other input controls whether data should be loaded in parallel or to be shifted. The output of OR gate is connected to input of next FF. This OR gate allows either Parallel load or shift data.

![Diagram of Shift Register](image)

**Figure 7: Parallel In Serial Out Shift register**

This register consists of 4 D flip flops. All flip flops are triggered simultaneously by a common clock. There are four parallel data inputs ABCD applied to the register. Parallel data bits and outputs of previous stage are given as inputs to two AND gates. Other input comes from direct control and inverted control as shown here. Outputs of the two AND gates act as inputs for the OR gate whose output is fed as input to the next stage of shift register as shown in figure 7.

Let us consider parallel data ABCD=0101. When the control line LOW, second AND gate is enabled and first AND is disabled. So parallel data bit appears as data input. Application of one clock pulse now allows this parallel data to be stored into the 4-bit register. Advantage of this configuration is that any number of bits are transferred into the register in a single clock pulse. With one clock pulse the parallel data available at D input appears at the output of register.

On the other hand, when control line is HIGH, first AND gate is enabled i.e. the Q output of previous FF appears as data input to the next stage. Here, four clock pulses are required to shift the data out of the register serially. The output of last FF Q3 acts as a serial data output of the shift register.

### 2.4 Parallel In Parallel Out (PIPO) shift register

In the 4 bit parallel in parallel out shift register, four independent D flip are used as shown in figure 8. The D inputs are acting as the parallel inputs and Q outputs of the FFs act as the parallel outputs of the shift register. Let us consider the parallel data ABCD = 0101.
The clock inputs of all FFs are triggered by a single clock signal. Once the register is clocked, all the data at the D inputs appear at corresponding Q outputs of the FFs simultaneously. This shift register requires only one clock pulse for operation; hence it is the fastest shift register.

3. Bidirectional shift register

It is the shift register in which the data can be shifted either left or right. The four bit bidirectional shift register using D flip flops is shown in figure 9. There are two AND gates and a OR gate used at the input of each D flip flop. This combinational circuit allows the serial data to be shifted left or right based on the Left/Right shift control pin.

Let us consider a binary data 1101 applied to the serial data in for left shift. The left'/Right input is set to 0. With this control input, the inverter produces 1 at the output which enables the second AND gates of the combinational circuit. This allows data present at second AND gate to pass through OR gate to D inputs of the FFs. The D input of FF4 receives the serial data; D input of FF3 receives Q3 output; D input of FF2 receives Q2 output and D input of FF1 receives Q1 output.
Application of a clock pulse shifts the data to the left by 1 bit position. After four clock pulses, the output of left shift register contains the data 1101. It further requires 3 clock pulses to shift the data out serially from Q0 of the left shift register.

Let us consider a binary data 0101 applied to the serial data in for right shift. The left’/Right input is set to 1. With this control input, the first AND gates of the combinational circuit is enabled. This allows data present at first AND gate to pass through OR gate to D inputs of the FFs. The D input of FF1 receives the serial data input; D input of FF2 receives Q0 output; D input of FF3 receives Q1 output and D input of FF4 receives Q2 output.

Application of a clock pulse shifts the data to the right by 1 bit position. After four clock pulses, the output of right shift register contains the data 0101. It further requires 3 clock pulses to shift the data out serially from Q3 of the right shift register.

4. Universal shift register

A universal shift register can transfer data in three different modes. It can load and transmit data in parallel. It can load and transmit data in serial fashion, through left shifts or right shift. This allows user to activate either SISO, SIPO, PISO and PIPO shift register. 4bit Universal shift register consist of 4 positive or negative edge triggered D flip flops. To load and transmit the data in parallel or serial fashion, there is a AND-OR combinational circuit at D input of every flip flop as shown in figure 10.

Figure 10: Universal shift register

Serial in or serial out can be implemented by shifting the data in any one of the two directions. Left shift requires Q0←Q1←Q2←Q3←serial Data in whereas the right shift requires Serial data in →Q0→ Q1→Q2→Q3.

For SISO, the shift in operation needs shift/load input connected to HIGH state and will take 4 clock pulses to shift the data serially in. The shift out operation also need shift/load input kept connected to HIGH state and will require 3 clock pulses shift data serially out. This is because the output already has LSB before shift out operation begins. For SIPO, the Shift/load operation is connected at HIGH state and will require no clock pulse to take the data is already available at the outputs.
<table>
<thead>
<tr>
<th>Type</th>
<th>Shift In</th>
<th></th>
<th>Shift Out</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Shift/Load</td>
<td>Number Of Clock Pulses</td>
<td>Shift/Load</td>
</tr>
<tr>
<td>Right shift</td>
<td></td>
<td>SISO</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SIPO</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PISO</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PIPO</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Left shift</td>
<td></td>
<td>SISO</td>
<td>0</td>
<td>4</td>
</tr>
</tbody>
</table>

**Figure 11: Functional table for universal shift register**

For PISO operation, shift/load input be connected to LOW state to enable parallel load operation. For shift out operation, the shift/load input must be connected to HIGH state for shift serial OUT and will require 3 pulses again. For PIPO operation, shift/load input be connected to LOW state to enable parallel load operation and requires only 1 clock pulse to load the data in parallel and no clock pulse to take the data at output since it is always available at the output.

For shift left operation, parallel data input (Dn) receives Qn+1 output, hence shift/load be connected to low state for both modes.

**5. Ring counter**

Ring counter is a type of shift register with the output of the last flip flop is fed back to the input of the first flip flop. The data stored within the shift register will circulate as long as clock pulses are applied. The 4-bit ring counter consists of four D flip flops with clock input connected to the common clock. External RESET input is connected to Preset input of the first FF and Clear input of all remaining flip flops as shown in figure 12.

![Ring counter diagram](image)

**Figure 12: Ring counter**

Let us understand the working of ring counter with the help of function table. Initially, an active LOW level is applied to Reset input, which sets Q0 as 1 and other flip flop outputs will be 0. The contents of the register are Q0Q1Q2Q3 =1000 as shown in figure 13.
Application of first clock pulse shifts the logic 1 to Q1 as D input of second FF is connected to Q0. The register now contains 0100. Application of second clock pulse shifts the logic 1 to Q2 as D input of third FF is connected to Q1. The register now contains 0010. Further application of third clock pulse shifts the logic 1 to Q3 as D input of fourth FF connected to Q2. The register now contains 0001. Forth clock pulse shifts the logic 1 to Q0 as D input of fourth FF connected to Q3. The register now contains 1000 again and ring counter operation continues further.

6. Johnson counter
A Johnson counter is a modified ring counter in which the complemented output of the last flip flop is connected to the input of the first flip flop. Johnson counter is also called as twisted ring counter.

Let us consider a 4-bit Johnson counter constructed using 4-D flip flops as shown in figure 14. The circular connection is made from complement output of the rightmost flip flop to the input of the leftmost D flip flop. The register shifts its contents one bit position to the right with every clock pulse and the complement value of last flip flop is transferred to the first flip flop at the same time.

Let us understand the working of Johnson counter. Initially, an active LOW level is applied to the clear input, which resets all the flip flops. Thus the register contains Q0Q1Q2Q3 =0000. With the first clock pulse, the first flip flop inserts 1 into the register as Q3’=1. The content of
the counter are 1000. With the second clock pulse, new ‘1’ is added into the register as Q3=1. The content of the counter is now 1100. Next clock pulse generates the counter contents as 1110. Fourth clock pulse shifts the whole contents to right and adds 1 to the left position. Thus we get 1111 as shown in figure 15.

<table>
<thead>
<tr>
<th>Clock pulse</th>
<th>Q0</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Figure 15: Operation of Johnson counter

As Q3=1, the complement of Q3 is 0. Now the value ‘0’ is inserted into the register. Thus, with the next clock pulse, the counter contains 0111. Next counter becomes 0011 with next clock pulse. Further it becomes 0001 with the clock pulse. Finally the counter becomes 0000 with the clock pulse.

Starting from the clear state, the Johnson counter goes through a sequence of 8 states. In general, a n-bit twisted ring Johnson counter will go through a sequence of 2xn states. The disadvantage of Johnson counter is that it does not count in binary sequence.

7. Shift register ICs

There are several commercially available shift register ICs. These include right from simple serial in serial out shift register to universal shift register IC under TTL logic family as shown in figure 16.

<table>
<thead>
<tr>
<th>IC</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7491</td>
<td>8 bit serial in / serial out shift register</td>
</tr>
<tr>
<td>7495</td>
<td>4-bit serial/parallel access shift register (Universal)</td>
</tr>
<tr>
<td>74164</td>
<td>8 bit serial in / parallel out shift register</td>
</tr>
<tr>
<td>74165</td>
<td>8 bit parallel load shift register</td>
</tr>
<tr>
<td>74166</td>
<td>8 bit parallel in serial out shift register</td>
</tr>
<tr>
<td>74174</td>
<td>6-bit parallel in parallel out shift register</td>
</tr>
<tr>
<td>74194</td>
<td>4 bit bidirectional universal shift register</td>
</tr>
<tr>
<td>74198</td>
<td>8 bit bidirectional universal shift register</td>
</tr>
</tbody>
</table>

Figure 16: Table showing commercially available shift register ICs.
8. Applications of shift registers

Shift register are used in variety of applications as listed below.
1. **Delay line**- The SISO register can be used to introduce time delay. The delay is proportional to number of flip flops.
2. **Serial to parallel converter**- Serial in parallel out (SIPO) shift register can be used to convert data in serial form to parallel form e.g. keyboard interfacing.
3. **Parallel to serial converter**- A parallel in serial out (PISO) shift register can be used to convert data in parallel form to serial form. This is required in a situation where parallel data transmission is not feasible at long distance e.g. modem/router interfacing.
4. **Sequence generator**- sequence to operate various electronic gadgets can be obtained using shift register
5. **Ring counter** - a particular set of control signals can be generated using ring counter.
Shift register is also used in
6. **Pulse train generator**
7. **Registers in processors**
8. **Keyboard encoding**
9. **Rolling display**
10. **Universal asynchronous receiver transmitter (UART)**

Let us now conclude this module by summarizing the important points in shift register.

9. Summary

Shift registers are basically a sequential logic circuit capable of storing binary data. The data can be accepted either in serial or parallel fashion and similarly transfer the data either in serial or parallel format. There are four basic types of shift registers: SISO, SIPO, PISO, PIPO. Shift register are mainly constructed using either SR, JK or D flip flop. Bidirectional shift register can move the data either to left or right direction serially. Universal shift register is capable of performing all these data transfer capabilities. The Ring and Johnson counter are special shift registers. The ring counter has n states in sequence whereas Johnson counter has 2n states in the sequence.
## Development Team

<table>
<thead>
<tr>
<th>Role</th>
<th>Name</th>
<th>Institution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Principal Investigator</td>
<td>Prof. A. D. Shaligram</td>
<td>Savitribai Phule Pune University, Pune</td>
</tr>
<tr>
<td>Paper Coordinator</td>
<td>Dr. N. M. Kulkarni</td>
<td>Fergusson College, Pune</td>
</tr>
<tr>
<td>Content Writer</td>
<td>Dr. N. M. Kulkarni</td>
<td>Fergusson College, Pune</td>
</tr>
<tr>
<td>Content Reviewer</td>
<td>Prof. D. B. Gaikwad</td>
<td>Modern College, Pune</td>
</tr>
</tbody>
</table>