Module -29

Programmable Logic Devices

Learning Objectives:

1. To understand new technology called as PLD.
2. To know the basic concepts of PLD
3. To explore types of PLDs.

1. Introduction

Most popular digital ICs were TTL logic family (74xxx series) till 2000 at least in India. Today they are hardly used in industrial applications. They are used only in education field for learning the concepts of digital electronics. They are very rapidly replaced by new kind of devices called as **Programmable Logic Devices** (in short PLDs)

74xx and other contemporary ICs are fixed function ICs. Normally they are SSI (small scale integration) and MSI (Medium scale integration) chips. Once the function is implemented by manufacturer it can never be changed. Whereas in PLDs the logic function is programmed by the user. So if the user wants he can reprogram the device number of times. Hence these ICs are called PLDs. Today PLDs are used extensively in industry and 74xxx ICs are used only in our education field.

For programming PLDs the user needs to know the features of Hardware Description Language (HDL). Either VHDL or VERILOG is used for programming PLDs.

2. Types of PLDs:

Programmable logic devices are mainly of three types. These are classified according to the complexity in design.

1. SPLD (**S**imple **P**rogrammable **L**ogic **D**evice)
2. CPLD (**C**omplex **P**rogrammable **L**ogic **D**evice)
3. FPGA (**F**ield **P**rogrammable **G**ate **A**rray)

3. Construction of PLDs:

All PLDs consist of programmable arrays. An array is essentially a grid of conductors forming rows and columns with fusible links at each cross point (similar to matrix of diode at each cross point). Arrays are of fixed type or programmable type. PLD consists of an OR array and AND array.

3.1 The OR array:

Construction of OR array is depicted in figure 1.It consist of matrix of rows and columns and number of OR gates. The rows and columns are interconnected with help of fusible links. In the beginning all the links are closed. Selectively some of these links are open and others are retained. This is called as programming the array. The matrix connections of two dimensional structures are given to the OR gates. In a row to connect the desired input to the OR gate only one fuse is left intact. The other links are open. Vertically to the columns the inputs and their compliments are connected (A, A', B, B'). This process of programming is carried out till the last row. The equations are then implemented by an OR array.

For example if the equation to be implemented is X1= A + B then A is selected on row1 and B is selected on row2 so OR gate implements A+B. Similarly other expressions are implemented by using other rows and columns and other OR gates.

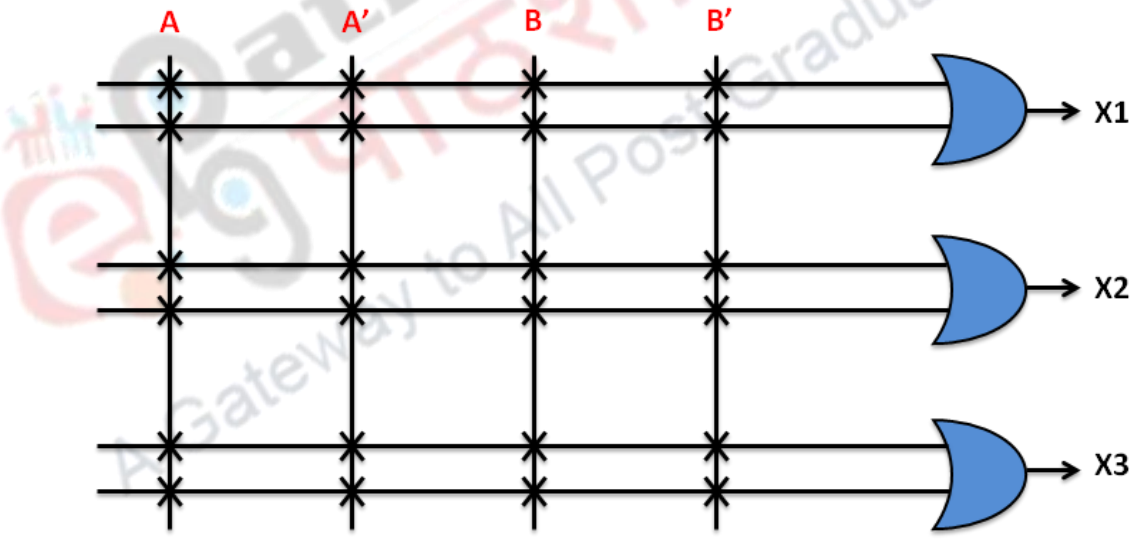

Figure1: Logic diagram of OR array with six rows and four columns

X = programming to be done

After Programming:

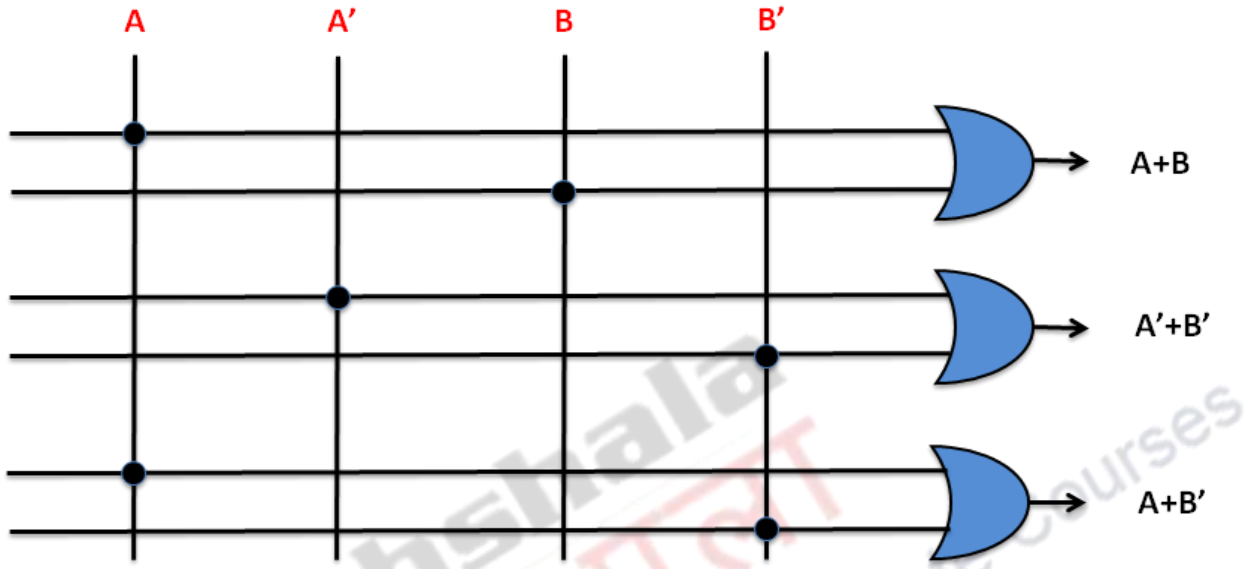

Figure 2: An OR array after programming

● = Connection is done.

Equations Implemented:

1. X1=A+B
2. X2=A'+B'
3. X3=A+B'

NOTE: Cross indicates programming to be done and dot indicates programmed connection.

As discuss earlier the OR array consists of an array of OR gates connected to programmable matrix with fusible links at each cross point of a row and column. The OR array is programmed by blowing the fuses to eliminate the variables and retain only one connection in a row. Therefore for each i/p to OR gate only one fuse is left intact in order to connect the desired variable to the gate i/p. Once the fuse is blown it cannot be reconnected.

Note : Another method of programming a PLD is to use antifuse. It is opposite to fuse. In this normally open contact is shorted by melting the antifuse material to form a contact or short a connection. Other places are left open.

3.2 The AND Array

Construction of AND array is depicted in Figure3.It consist of matrix of rows and columns and number of AND gates. The rows and columns are interconnected with help of fusible links. In the beginning all the links are closed. Selectively some of these links are open and others are retained. This is called as programming the array. The matrix connections of two dimensional structures are given to the AND gates. In a row to connect the desired input to the AND gate only one fuse is left intact. The other links are open. Vertically to the columns the inputs and their compliments are connected (A, A', B, B'). This process of programming is carried out till the last row. The equations are then implemented by an OR array.

For example if the equation to be implemented is X1= A . B then A is selected on row1 and B is selected on row2 so AND gate implements A+B. Similarly other expressions are implemented by using other rows and columns and other AND gates.

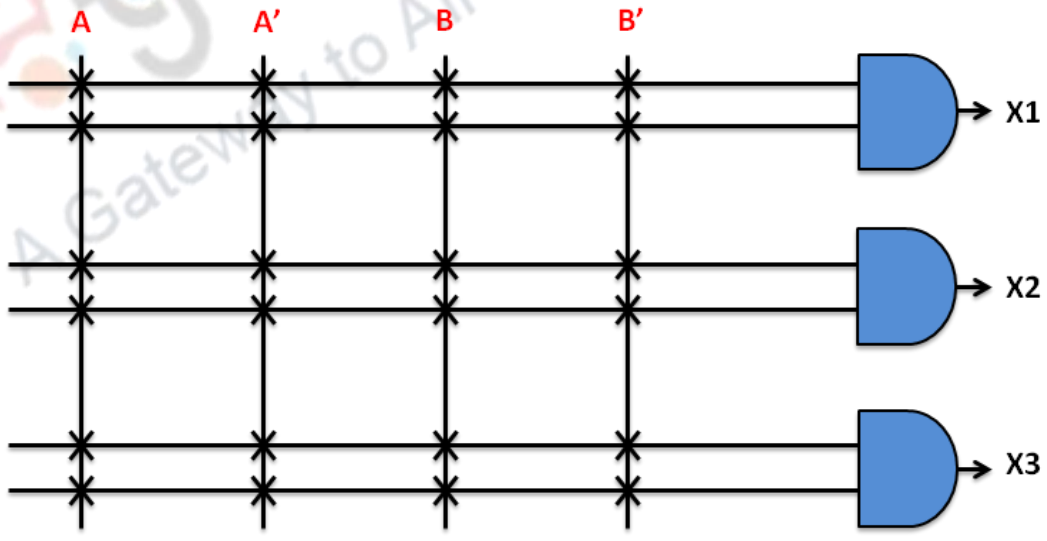

Figure3: Logic diagram of AND array with six rows and four columns

X = programming to be done

After programming:

Equations Implemented:

1. X1=A. B
2. X2=A'. B'
3. X3=A. B'

NOTE: Cross indicates programming to be done and dot indicates programmed connection.

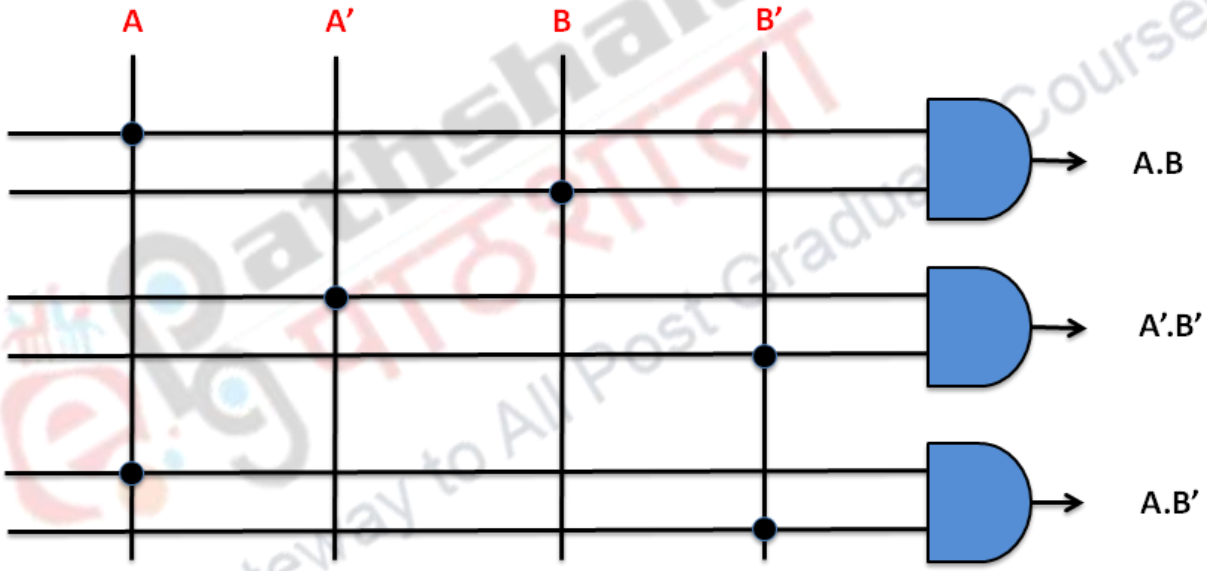

Figure 4: An AND array after programming

● = Connection is done.

As discuss earlier the AND array consists of an array of AND gates connected to programmable matrix with fusible links at each cross point of a row and column. The AND array is programmed by blowing the fuses to eliminate the variables and retain only one connection in a row. Therefore for each i/p to AND gate only one fuse is left intact in order to connect the desired variable to the gate i/p. Once the fuse is blown it cannot be reconnected.

4. Types of SPLD:

All the programmable basically carry combination of OR array and AND array. With the help of the links different programming devices are obtain. Basically it implements SOP (**S**um **O**f the **P**roducts) types expressions. Depending upon ability of programming the SPLDs are of the following types:

1. PROM (Programmable Read Only Memory)
2. PLA (Programmable Logic Array)
3. PAL (Programmable Array Logic)
4. GAL (Generic Array Logic)

PROM:

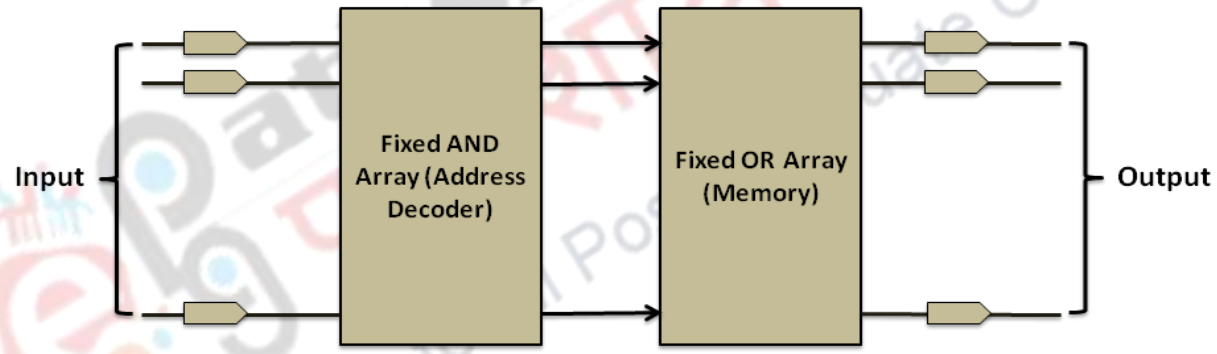

Figure 5: Block diagram of PROM

It consists of fixed or nonprogrammable AND array connected as address decoder and programmable OR array as a memory.

Example: i) 28C64 → 8Kx8 → 8Kbyte

ii) 28C256 → 32Kx8 → 32Kbyte

iii) 28C010 → 128Kx8 → 128Kbyte

iv) 28C040 → 512Kx8 → 512Kbyte

Pin diagram of 28C64 ⟶ 28 pin, 8K x8, PROM

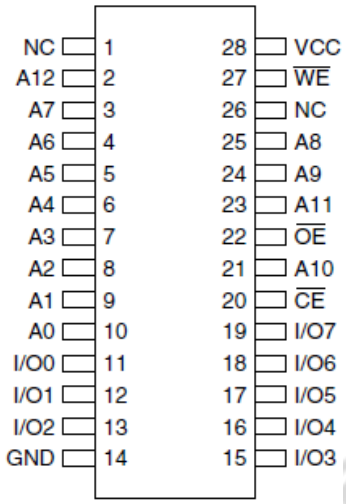

Figure 6: Pin diagram of 28C64 Memory (Courtesy: Intel cor.)

2. PLA:

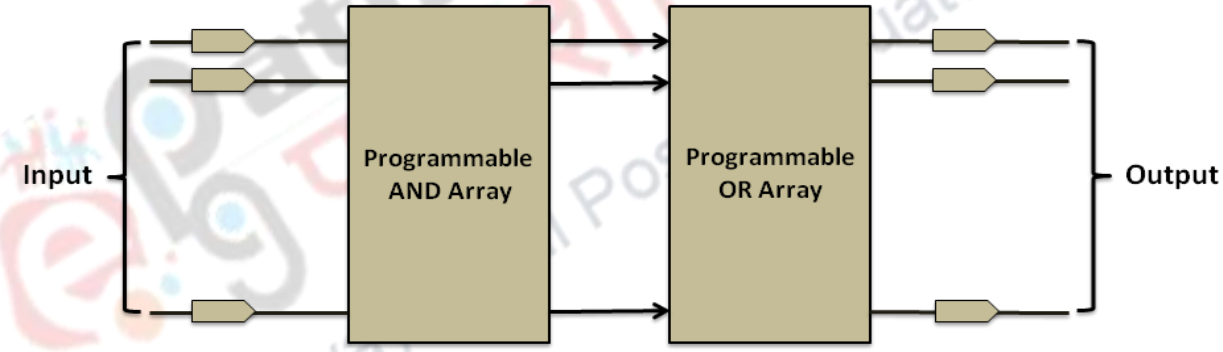

Figure 7: Block diagram of PLA

It consists of a programmable AND array and programmable OR array. It is also called FPLA (field programmable logic array). Because, it is programmed by user. It is not programmed by manufacturer. E.g. Signetics: 82S100. It is introduced in 1974 having 16 inputs and 8 outputs. It has 48 AND gates in AND array and 8 OR gates in OR array. It has 2x16x48=1536 fuses in AND array and 8x48=384 fuses in OR array.

3. PAL:

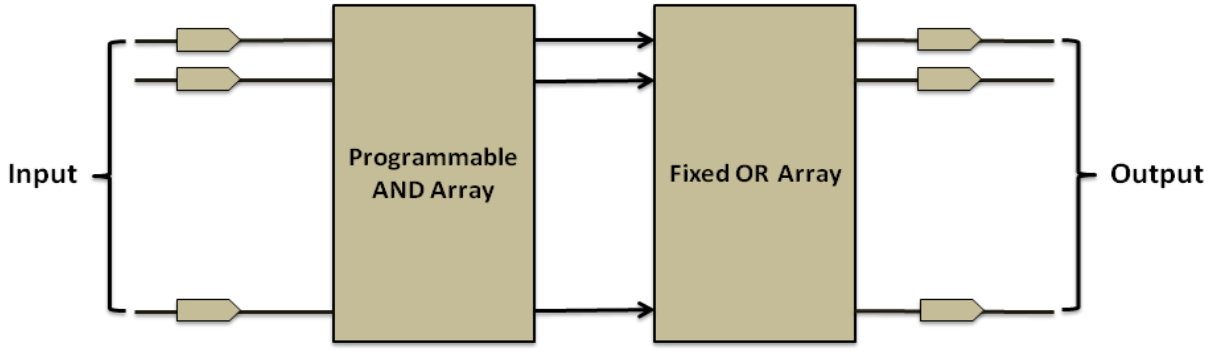

Figure 8: Block diagram of PAL

It consists of programmable AND array and fixed OR array with output logic. It is OTP. i.e. one time programmable device. It is implemented by using TTL or ECL technology. e.g. PAL16L8; PAL20L8; PAL12H6; PAL10P8; PAL10L8.

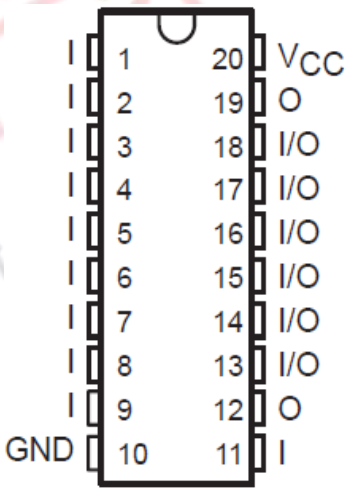

Figure 9: Pin Diagram of PAL 16L8 (Courtesy: Intel cor.)

4. GAL:

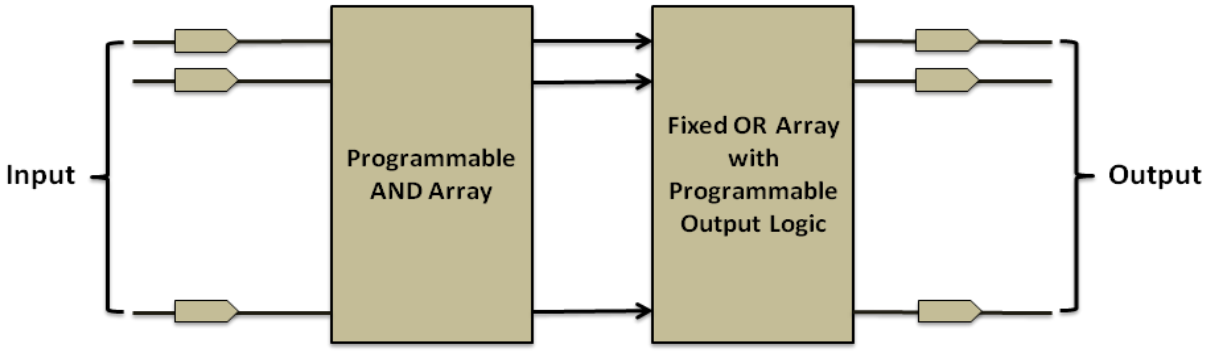

Figure 10: Block diagram of GAL

It has reprogrammable AND array and fixed OR array with programmable output logic. It uses E^2CMOS technology or floating gate technology. Therefore it is generic and so many other PAL like structures can be developed.

e.g. GAL18V6; GAL16V8C; PALCE20V8

Note that these ICs have changed the size of the electronic products. Because if the same circuits are to be realized by using fix function ICs then it takes lot of spaces. It's very bulcky.but with PLDs these product is very light in weight. Using these technologies custom or semi custom IC's were manufactured. Such IC's are called as ASICs (Application **S**pecific **I**ntegrated **C**ircuits).

ASIC:

There are many manufacturers of PLDs. So they are available as of the shelf components (Like we buy medicines). As they are programmable most logic circuits in digital hardware can be implemented using them. But the problems with these PLDs are that they consume lot of chip area. Also the speed of operation is less because of programmable switches or connections. So they are cost effective and they may not give desired performances. In such cases or when the digital products are required in large number, a different approach of ASIC is taken.

In this approach the digital products is designed by a chip that implements the desired logic circuits. Then the appropriate technology is selected. The chip is then outsourced for manufacturing to a company that has the fabrication facilities. This chip is then used in digital products for a specific application. Such chips are called ASICs.

ASICs are customs chip because they are used only in one particular application they cannot be used for the general purpose applications.

Advantages:

1. It is designed to optimize the specific task so it gives the best performance.
2. It is possible to put large amount of logic circuitry in a single chip
3. As these ICs are produced in bulk, cost of the manufacture per chip is very low. So the cost per chip is far less than the fixed function ICs.
4. They can be used in embedded systems.

Disadvantage:

It takes considerably long time to manufacture ASIC or custom chip. But only one or two products are required then PLDs are best.

PLD Programming:

PLD need to be programmed by an expert designer. He needs to know how to programs these ICs by using one of the hardware description languages (HDLs). Fixed function IC designer need not to know HDL. This can be disadvantage (if one thinks so).

Logic circuit design for PLDs is entered using computer by two methods.

1. Schematic Entry
2. Text Base Entry

In schematic entry the software permits the user to enter the symbols to logic gates, flip flops and also to interconnect them. On the screen a schematic diagram similar to logic diagram is seen.

In text based entry, the software permits the user to enter the design by using a text of HDL. For this either ABEL (**A**dvanced **B**oolean **E**xpression **L**anguage), CUPL (Complier for **U**niversal **P**rogrammable **L**ogic) , VHDL(**V**ery high Speed **H**ardware **D**escription **L**anguage) or Verilog can be used as language.

PLD design is simulated on the screen using one the above techniques. If simulation works fine then the implementation of the design is done on PLD.This is done by using an ADDON unit to a computer where the PLD is burnt. Later on it is used in real products.

Summary:

ICs are of two types: fixed function and Programmable ICs.

Function of Programmable logic devices (PLDs) can be changed through programming

There are three types of PLDs: SPLD, CPLD and FPGA.

All PLDs consist of programmable arrays. Arrays are of fixed type or programmable type. PLD consists of an OR array and AND array.

SPLDs are classified as PROM, PLA, PAL and GAL.

ASICs are customs chip because they are used only in one particular application they cannot be used for the general purpose applications.