Module-19

Counters

Learning Objectives:

1. To understand the operation of asynchronous and synchronous counters
2. To construct simple up/down counters
3. To learn to use modulus counters.
4. To study of commercially available counter ICs

1. Introduction

Counting is frequently required in computers and other digital system for recording number of events. Normally all digital counters, count the number of pulses at the input in a specified time period. They must possess memory as it has to remember its past count or value. Flip flops can be used for storing the binary information. One of the popular applications of flip flops is counting the pulses and events. Counters can also be used for measuring frequency as well as time.

Counters are popularly used for timing, sequencing and counting applications. While designing a digital clock, a high frequency square wave say around 1MHz is available and it is necessary to generate 1Hz frequency. In this case, counter can be used as frequency divider to generate precise clock frequency. Similarly, it is important to activate different stage of the rocket in a proper sequence for launching the satellite. In such a case, counters are normally used to generate a predetermined sequence of binary numbers. For smart cities, it is necessary to have a smart traffic control system wherein it is necessary to measure the traffic flow on the roads. For measuring the number of vehicles automatically, a binary counter is triggered by a photo-sensor to increment the tally of vehicles.

Counters are very widely used component in digital systems and usually manufactured as a separate MSI -IC or a part of larger and complex IC. In this module, the basic principles and applications of counters will be explored.

2. Basic digital counter-

A counter is basically a sequential circuit that goes through a predetermined sequence of binary states. It counts in binary from 0 to 2^n-1, where n is the number of flip flops. The output value of counter increases by one on each clock cycle. After the largest value, the output of a counter "wraps around" back to 0.

Figure-1 shows the basic a generalized representation of a digital counter. Counter in its basic form accepts a clock input and produces a multi-bit binary output. The binary count is related to the total number of clock pulses applied to the clock input.

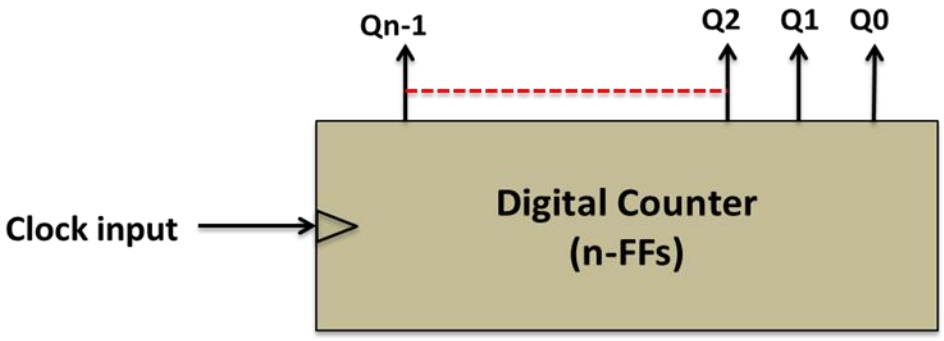


Figure 1: Basic digital counter

A multi-bit binary value of a counter at a given time is called as the state of the counter. The maximum number of states that a counter may have is limited by the number of flip flops. A count sequence specifies the exact order in which the output states will appear. Usually, the count sequence is cyclic in nature as shown in figure 2. In certain counters, it is possible to load or clear the count sequence at any time. To implement this feature in the counter, external inputs like Load or Clear' are additionally provided. Some binary counters provide additional input "up-down" control input to determine the direction of binary count sequence.

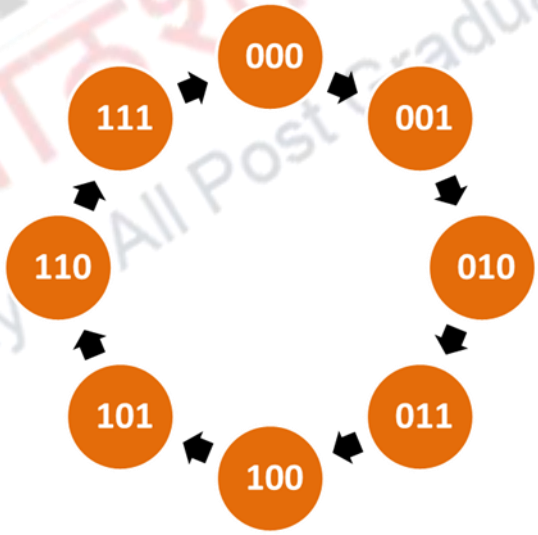


Figure -2: Count sequence for 3-bit binary counter

Flips flops can be connected together to perform counting action. The number of flip flops used in the circuit can decide the maximum count for a counter. There are different ways to classify the counters based on distinctive characteristics as shown in figure 3.

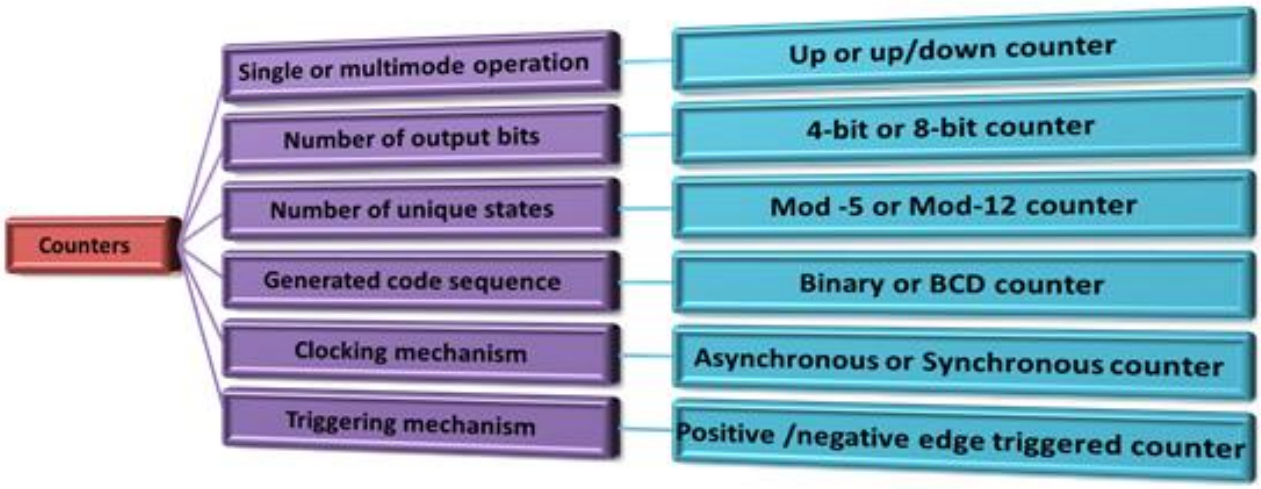


Figure 3: Classification of counters

Counters are usually built with the cascaded interconnection of flip flops. Each flip flop is operating in the toggle mode. The number of flip flops in a counter decides the counting capability of a counter. For example, one flip flop counts up to 2, two flip flops counts up to 4, three flip flop counts up to 8, four flip flops counts up to 16 states and so on…… In the generalized form, counter with **n** flip flops, can count up to $\mathbf{2^n}$ states. Figure 4 indicates the basic JK flip flop as the basic counting element operated in toggle mode.

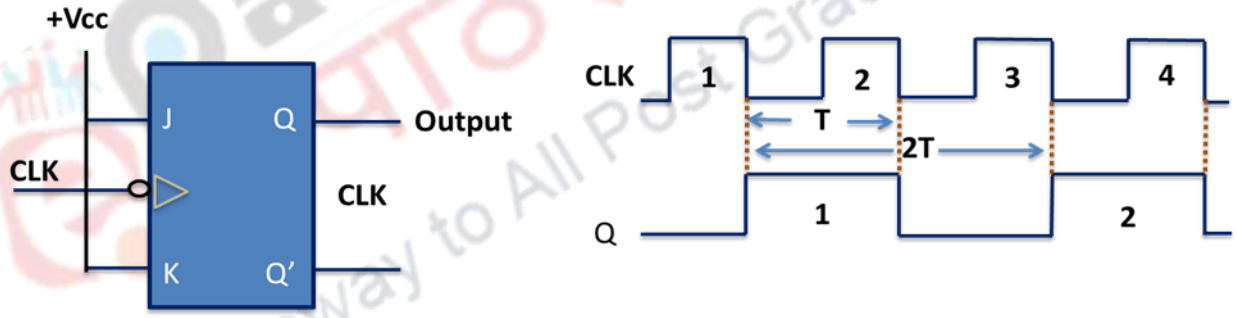


Figure-4: JK flip flop as basic element of counter

To operate JK flip flop in a toggle mode, the J and K inputs are connected to +Vcc i.e. at logic 1 and square wave with frequency f is applied to the clock input. The Q output of the flip flop toggles i.e. changes the state at negative or falling edge of the clock. Referring to the timing diagram, with every falling edge of the clock, the output changes the state. This results in new pulse train with double the period of the original clock and thus provides 2 pulses. Now, it is possible to conclude that one flip flop in a toggle mode provide **divide by 2**action where the input clock frequency is divided by 2. If this output is given to the next flip flop, the output gives further division by 2 and the process can be continued for any number of flip flops.

3. Asynchronous (Ripple) counter

An asynchronous counter is the one where only the first flip flop is given the external clock. All subsequent flip flops are clocked by the output of preceding flip flop. Asynchronous counters are also called ripple counters because of the way the clock pulse travels or ripples through the flip flops. Asynchronous counters are slower than synchronous counters because of the delay in the transmission of pulses for one flip flop to another. With a synchronous counter, all the flip flops in the circuit change in synchronism with the input clock.

There are many ways to implement the ripple counter depending upon the characteristics of the flip flop used like the clock trigger, JK or D flip flop and count direction – up or down.

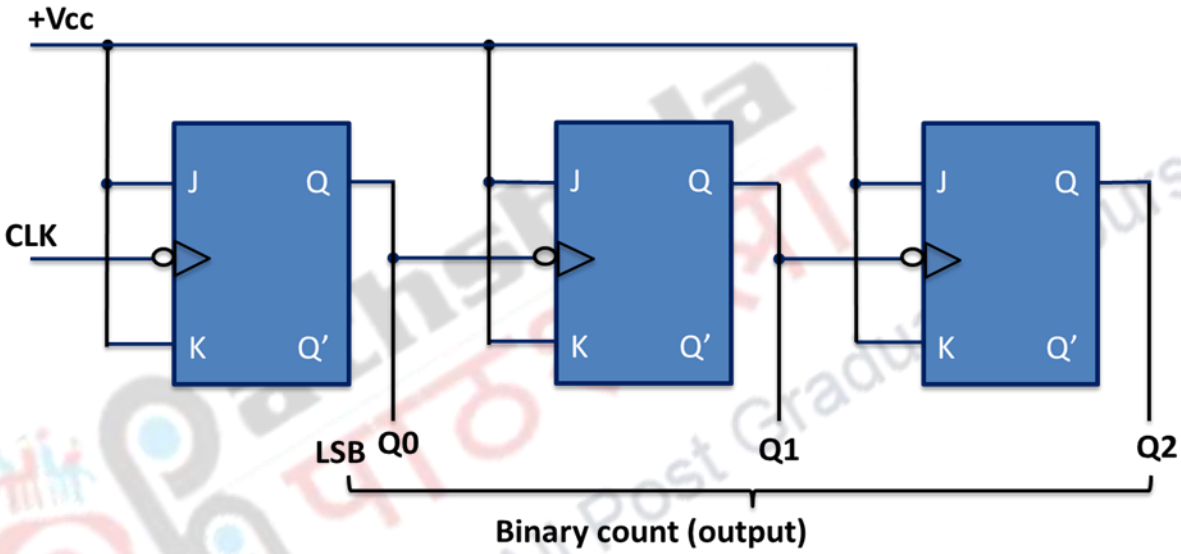


Figure 5: Asynchronous or Ripple counter (up counter)

For a 3-bit counter, three negative edge triggered JK flip flops are connected to +Vcc to operate them in toggle mode as shown in figure 5. In a ripple counter, all the flip flops are connected in cascade. The input clock is connected to first JK flip flop. The output Q0 of the first flip flop drives the clock input of the second flip flop.The output Q1 of the second flip flop drives the clock input of the third flip flop. The last JK flip flop output generates Q2 i.e. MSB of the counter. When the output of a flip flop is used as the clock input for the next flip flop then it is called as ripple or asynchronous flip flop. The output of the ripple counter is Q2 Q1 Q0 written as per the binary sequence.

The timing diagram of the ripple counter is shown in figure 6. Clock input is the square wave which drives the first flip flop. All the outputs of the counter are written in the following starting with Q0, Q1 and finally Q2. Let us begin with reset condition of the counter. The counter output is 000.

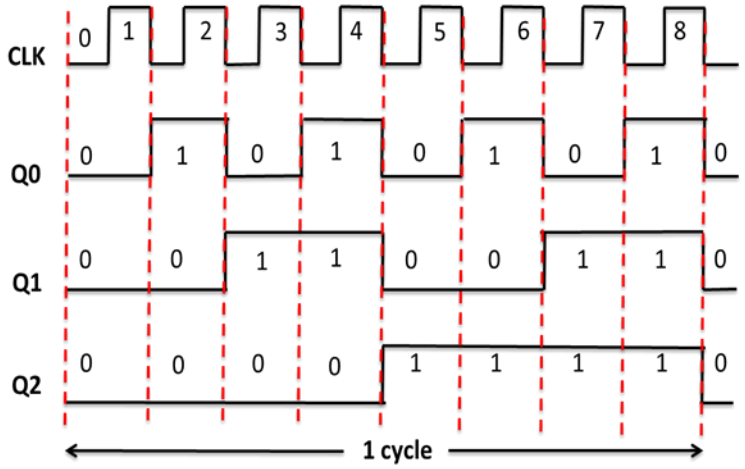


Figure 6: Timing diagram of Ripple counter

All the JK flip flops will change the state at the negative edge of the its clock input. With the negative edge of the clock input, the output of the first flip flop Q0 changes the state from 0 to 1.The counter output becomes 001. As soon as clock makes the second negative transition, the output of first flip flop changes the state from 1 to 0. The negative state change at Q0 triggers second flip flop, which forces the output to change the state from 0 to 1. The binary count is now 010. With the next negative clock transition Q0 changes the state from 0 to 1.And the counter increments to 011. The fourth clock transition forces Q0 to change the state from 1 to 0. The negative transition triggers second flip flop and it changes the state from 1 to 0. The negative going transition triggers last flip flop for the first time and the output Q2 changes 0 to 1. The binary count is now 100. With the next clock transition Q0 changes the state from 0 to 1.The count further becomes 101. With the next negative transition at clock pulse, Q0 changes the state from 1 to 0, Q1 changes the state 0 to 1 and Q2 remains at 1.This generates the next binary count as 110. With the next clock transition Q0 once again changes the state from 0 to 1 and Q1 and Q2 outputs remains unchanged.The output of the counter is now 111. With the next clock transition, all flip flops change their states from 1 to 0. Thus the counter resets back to the count 000.

Let us sum up the operation of binary ripple counter. First flip flop changes the state at every negative transition of the clock. Note that the waveform at the output Q0 is one half the clock frequency. Output Q0 acts as the clock for second flip flop. This flip flop toggles at each negative transition of the Q0. Note that the waveform at the output Q1 of second flip flop is one half the frequency of Q0 or one fourth the clock frequency.The output Q1 of second flip flop acts as a clock input to third flip flop. The negative edge transition of Q1 toggles the state of third flip flop. The frequency at output Q2 is one half the frequency at output Q1 and one eighth the clock frequency.

Down Counter

To construct a 3-bit down counter, three negative edge triggered JK flip flops are connected to +Vcc as shown in figure 7. In a ripple counter, all the flip flops are connected in cascade. The input clock is connected to first JK flip flop. There is one change, the complement of the output of first

flip flop i.e. Q0' of the first flip flop drives the clock input of the second flip flop.Similarly, the complement of the output of second flip flop i.e. Q1' drives the clock input of the third flip flop.

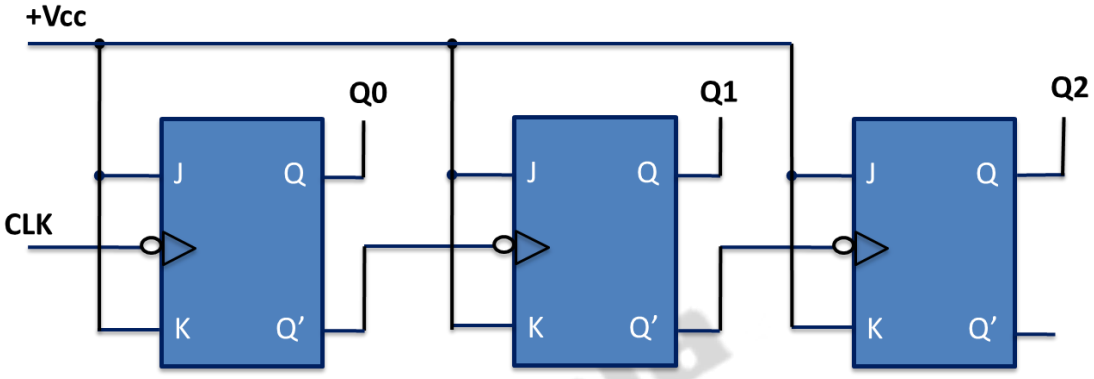


Figure 7: Asynchronous down counter

The timing diagram of the ripple down counter is shown in figure 8. Clock input is the square wave which drives the first flip flop. All the outputs of the counter are written in the following starting with Q0, Q1 and finally Q2. Let us begin with reset condition of the counter. The counter output is 000. It is important to note that complement of outputs Q2'Q1'Q0' are 111.

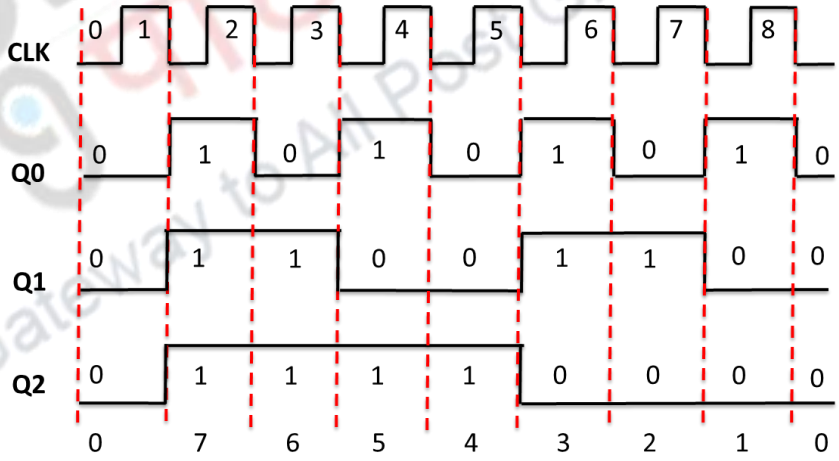


Figure 8: Timing diagram of down counter

All the JK flip flops will change the state at the negative edge of the its clock input. With the first negative edge transition of the clock input, the output of the first flip flop Q0 changes the state from 0 to 1. The complement of output of first flip flop Q0' goes from 1 to 0 which drives clock input of second flip flop. Thus second flip flop output Q1 also changes the state from 0 to 1. The complement of output of second flip flop Q1' goes from 1 to 0 which drives the clock input of third flip flop. Thus, the third flip flop output Q2 changes state from 0 to 1.This provides the counter

output as 111 i.e. decimal 7. With the second negative clock transition, the Q0 changes the state from 1 to 0.

The counter state is now 110 i.e. decimal 6. The third negative clock transition changes the output Q0 from 0 to 1. With this Q0' provides negative edge for triggering second flip flop, which changes Q1 from 1 to 0.Counter now decrements to 101 i.e. 5. After fourth negative transition, Q0 changes from 1 to 0 and Q1 and Q2 are unchanged.Counter further decrements to 100. With fifth negative clock transition, Q0 changes from 0 to 1, which triggers second flip flop and to change the state of Q1 from 0 to 1. With Q1 changing from 0 to 1, Q1' changes from 1 to 0, which triggers third flip flop and it goes from 1 to 0.This forces the counter to decrement further i.e. 011 means decimal 3. The sixth clock transition changes the output Q0 from 1 to 0 and no change in Q1 and Q2.Counter now becomes 010 i.e. decimal 2. Now the seventh clock transition, once gain triggers first flip flop to change the output from 0 to 1, This makes Q0' to change the value from 1 to 0, which triggers second flip flop and Q1 changes from 1 to 0.The counter output is now 001 i.e. decimal 1. With the eighth negative transition, the output of first flip flop Q0 changes state from 1 to 0. This also keeps Q1 and Q2 in 0 states.Thus the down counter resets back to the state 000.

In binary down counter, the counter counts from 111 to 000 by decrementing by 1 with every clock transition.

Different methods to construct counters -

Parameter								
Types Of FFs (Edge Triggered)	Negative	Negative	Negative	Negative	Negative	Negative	Negative	Negative
Cascaded Outputs Used For Interconnection	Q	Q	Q'	Q'	Q	Q	Q'	Q'
Output Of Counter	Q	Q'	Q	Q'	Q	Q'	Q	Q'
Nature Of Counter(mode)	Up	Down	Down	Up	Down	Up	Up	Down

Figure 9: Table indicating various method of constructing counters

Let us now understand different methods to construct counters. There are three important parameters like Type of flip flop i.e. positive or negative edge triggering, cascaded output Q or Q' for interconnection, whether the output of counter is from Q or Q' outputs of the flip flops must be considered while implementing the counter. This table indicates eight different methods to construct counter. Let us consider first case of negative edge triggered flip flop, if we use Q output of previous flip flop as clock input of next flip flop for the cascading, it results in up counter at Q outputs. If we use Q' for cascading then the counter results in down counter and so on.

4. Up/Down counter

Some counters can have the facility of either counting up or down. To achieve this, we can use a combinational AND-OR circuits to pass Q or Q' for cascaded interconnections of the flip flops.Let us consider a simple 3-bit up/down counter. For such counter, let us consider three JK flip flops in toggle mode where the JK inputs are tied to +Vcc as shown in figure 10.

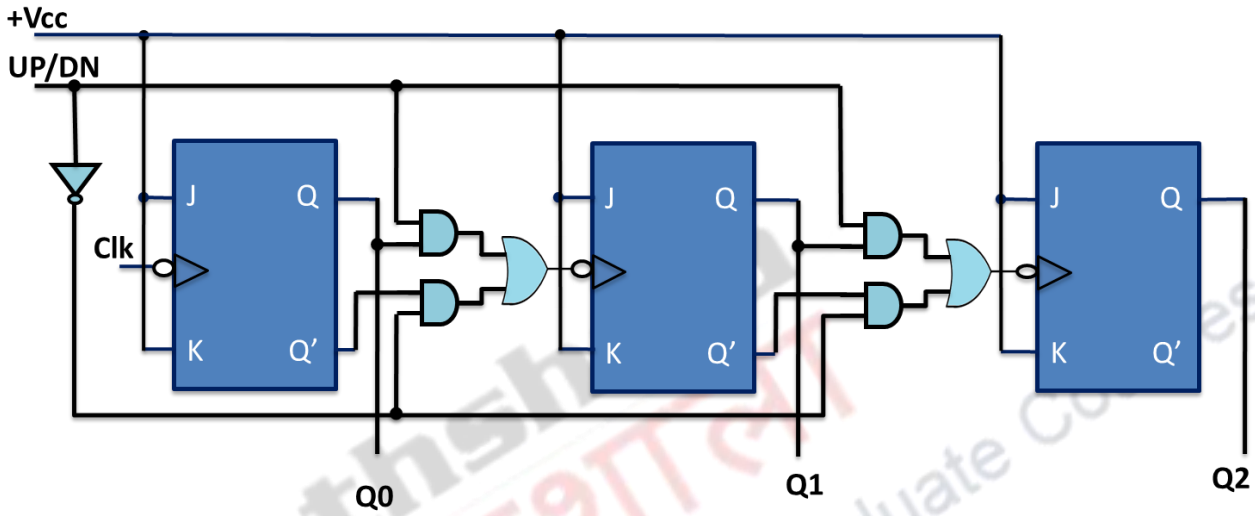


Figure -10: Binary up/down counter

A square wave pulse is applied to the clock input of the first flip flop. For up counting action, the Q output of previous stage is connected to the clock input of the next flip flop. Whereas for down counting action, the Q' output of the previous stage is connected to the clock input of the next flip flop. To have either up or down counting action an OR gate can be used at the clock input side. To enable only one type of counting at a time, the inputs to the OR gates are derived from AND gates.

A separate control input labeled as UP/DN' is introduced to enable only one type of counting either up or down at a given instant of time.When UP/DN' line is connected to HIGH state, the Q outputs are passed to the OR gate by enabling the upper AND gates and disabling the lower AND array. This sets up up counting mode for the counter. The counter counts up with every clock pulse. IT is also important to note that when UP/DN' is HI, count down line will be low due to use of inverter, which disables the lower AND gates.

Similarly, when UP/DN' line is low, the count down line is high. This enables lower array of AND gates, which allows Q' outputs of every stage to be connected to the clock input of next stage. Obviously, the counter is set in count down mode.

The binary output Q2 Q1 Q0 of the counter will be either counting up or down depending on the status of UP/DN'.

5. Effect of propagation delay in ripple counter

The problem with ripple counters is that each new stage put on the counter adds a delay. This propagation delay is seen when we look at a less idealized timing diagram. The output Q0 appears after some propagation delay as shown in figure 11.

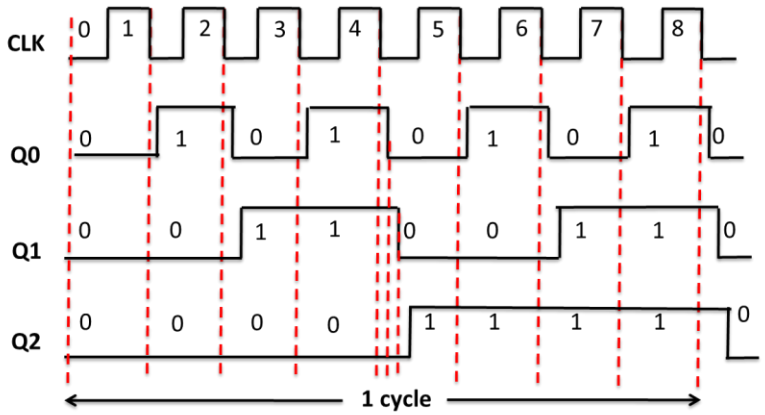


Figure 11: Effect of propagation delay

The second flip flop output Q1 is delayed by the two flip flop delay times as seen at fourth clock transition. This is applicable to every transition of the output Q2.Similarly after fourth clock transition, the flip flop output Q2 is delayed further by 3 flip flop delay times. It should be noted that the propagation delay does not only slow down the counter, but it actually introduces errors into the system. These errors increase as we add additional stages to the ripple counter.
A close-up look at this effect during several transition shows that there will be **false** output counts generated in the brief time period (called a glitch) and the "ripple" effect takes place.

6. Difference between asynchronous and synchronous counters

Now let us try to understand the difference between asynchronous and synchronous counters. There are six main parameters considered for comparison as shown in figure 12.

Parameters	Asynchronous counter	Synchronous counter
Clock input	Applied to first flip flop	Simultaneously to all flip flops
Cascading / Interconnection	Output of first flip flop is connected as clock to next flip flop.	Q outputs are connected either to JK inputs or ANDed with clock input
Type of FFs	Toggle flip flops are preferred	Any flip flop can be used.
Speed	Depends on no. of flip flops	Independent of no. of flip flops.
Additional circuitry	No extra logic gates are required, hence simple	Logic gates are required based on design & hence complex
Cost	Less	More

Figure 12: A table of comparison of asynchronous and Synchronous counters

7. Synchronous counters

In synchronous counter, all the flip flops are triggered by a common clock pulse as shown in fig.13. All flip flops are in toggle mode and triggered simultaneously, hence change the state simultaneously. Speed of synchronous counter is high as clock is given at a same time.

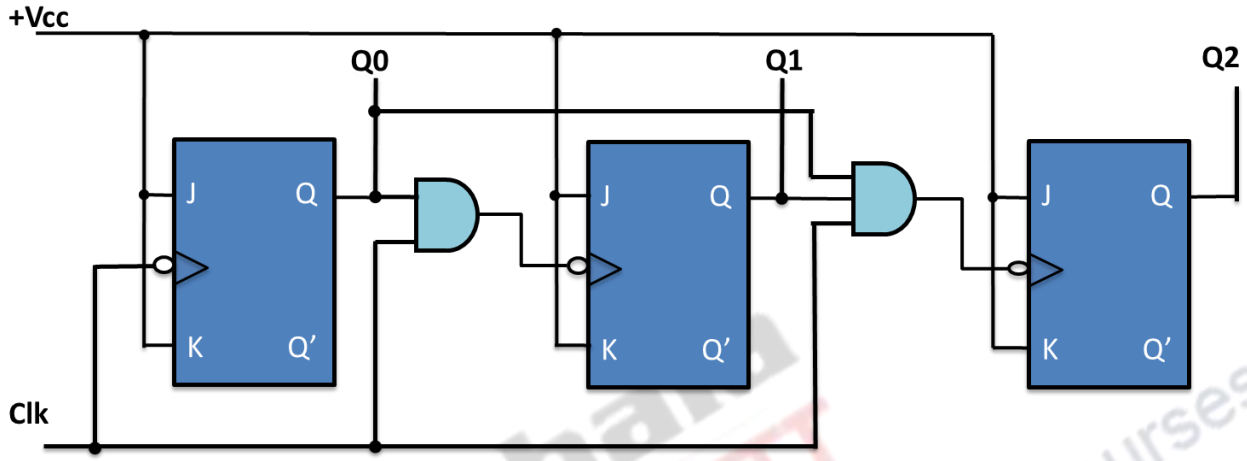
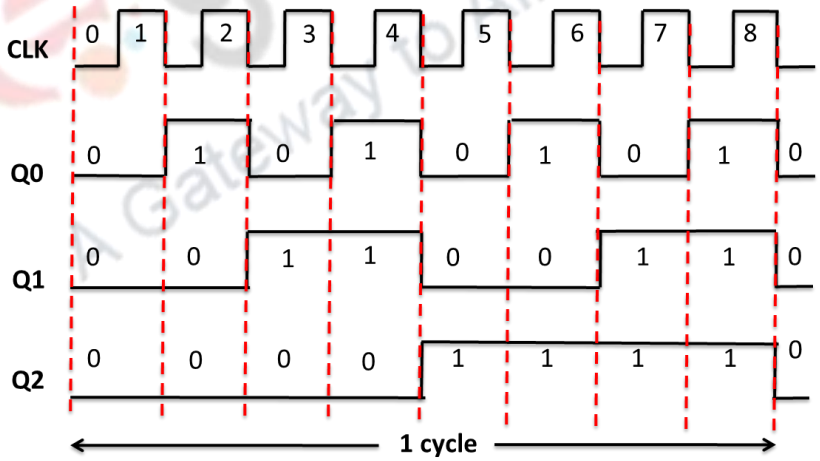


Figure 13: 3-bit synchronous counter

In synchronous counter the common clock pulse is simultaneously applied to all the flip flops. All flip flops will toggle with the negative transition of the clock pulse. The clock input reaches directly to first flip flop. The second flip flop triggers only when Q0 is high and common clock input makes the transition. AND gate is enabled at every second clock pulse whereas the third flip flop receives the clock only when both previous flip flop outputs Q1 and Q0 are at logic high. This logic configuration is popularly known as steering logic because the clock pulses are gated or steered to individual flip flop.



Q2	Q1	Q0	Count
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7
0	0	0	0

Figure 14: Timing diagram and count sequence for Synchronous counter

Let us discuss the working of the counter with the help of timing diagram as well as count sequence as shown in figure 14. Initially, the counter is in RESET condition. The first flip flop toggles with each negative transition of the clock and changes the state from 0 to 1 or 1 to 0.Whenever the first

flip flop output Q0 is HIGH, the AND gate is enabled and the clock pulse is passed through it to the clock input of the second flip flop. The second flip flop output Q1 changes the state at every second clock pulse. Third flip flop toggles only when both Q1 and Q0 outputs are at HIGH state, which enables the AND gate and passes the clock pulse. The third flip flop changes the state at every four clock pulse.

The visual inspection of the waveforms and truth table indicates that all the flip flops changes the states in synchronism and counter counts the natural binary up counting action from 000 to 111. After eight clock pulses, the counter resets to 0, hence this counter is also called as mod-8 counter.

8. Modulus counters

Modulus (MOD) is the number of states the counter counts in a complete cycle before it goes back to the initial state. A counter has a natural count of 2^n, where n is the number of flip flops in the counter. The number of flip flops used in the counter depends on the MOD of the counter. For example, two flip flops generates MOD-4 counter action, three flip flops generate MOD-8 counter action.

The counters are limited for counting MOD-2, MOD-4, MOD-8, MOD-16 etc. In many applications it is necessary that counter do not count all their possible states instead count up to m and then returns to zero. For example, MOD-3, MOD-5, MOD-6, MOD-10 counters. Modulus counters with modified count can be constructed in a synchronous, asynchronous or combination of both. One can even decide on which count can be skipped. Modulus counters are also called as **divide by n** circuit i.e. MOD-n circuit.

8.1 MOD-3 counter

A MOD-3 counter is the one where counter counts only three states. Let us consider a circuit consisting of two negative edge triggered JK flip flops as shown in figure 15. For the first flip flop J input is connected to Q' of the second flip flop and the output of first flip flop Q0 drives the J input of the second flip flop. The K inputs of both the flip flops are assumed to be at logic 1.

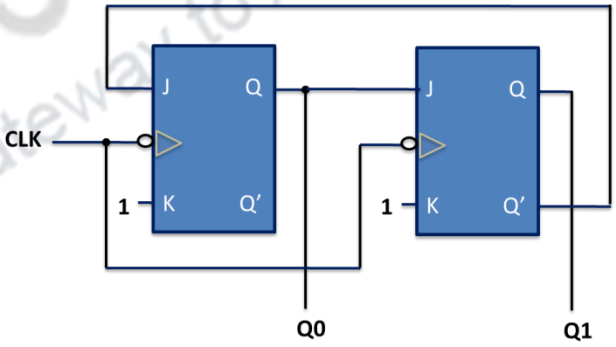
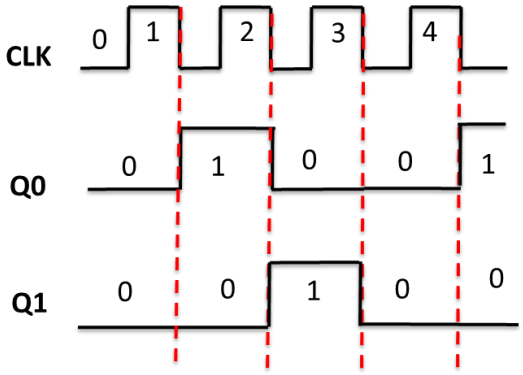


Figure 15: MOD-3 counter

Let us explain the working of MOD-3 counter using timing diagram and count sequence as shown in figure 16. Initially, the counter is assumed in the initial state i.e. 00. Now the J input of first flip is at 1 state since Q1' is 1 and K is also 1. Similarly, J input of second flip flop is 0. With the first negative transition of the clock first flip flop changes the state from 0 to 1 whereas second flip flop do not toggle. This generates next count as 01.



Q1	Q0	Count
0	0	0
0	1	1
1	0	2
0	0	0

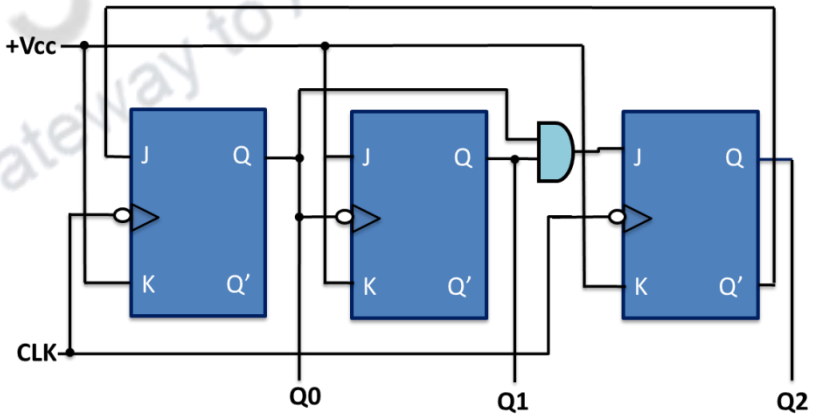
Figure 16: Timing diagram and count sequence for MOD-3 counter

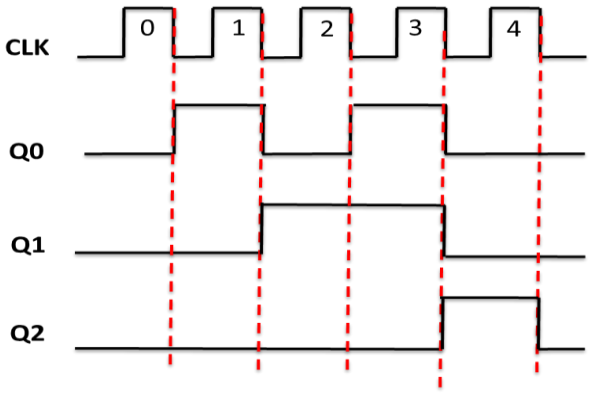
With the second clock transition, first flip flop once again toggles and changes the state from 1 to 0. Whereas second flip flop now toggles the state from 0 to 1, which generates the count 10. At this stage as Q1=1 means Q1'=0, which provide input J=0 for the first flip. Flop. Similarly, J input of second flip is also at 0 state since Q0=0. With the next clock, both the flip flops are in reset mode. This will generate a count sequence 00→01→10 and then back to 00.

8.2 MOD-5 counter

For MOD-5 counter, three flip flops are required with some truncated counts, since lowest natural count next is 8. Let us construct the circuit so that the counter begin counting with 000 and end with count 101.

The MOD-5 counter is constructed using three negative edge triggered JK Flip flops as shown in figure 17. The J input of first FF receives output Q' of the last FF and K is HIGH. This ensures that J remains HIGH for first four clock pulses (since Q' =1). Q of the first FF triggers the second FF. The third FF toggle only if Q1 and Q0 are in HIGH state. Hence AND gate is used to derive input for J input of third FF.





Q2	Q1	Q0	Count
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
0	0	0	0

Figure 17: MOD-5 counter with timing diagram and count sequence

The second FF triggers at the negative edge of Q0. Thus the second FF toggles only twice. The third FF changes state only when Q1Q0 =11 during fourth clock pulse. At this stage the counter produces a count 100, which provides the reset condition for the last FF on arrival of next clock pulse. This effectively produces a count 000. As this counter counts only 5 counts from 000→001→010→011→100 and resets back to 000.

8.3 MOD-6 Counter

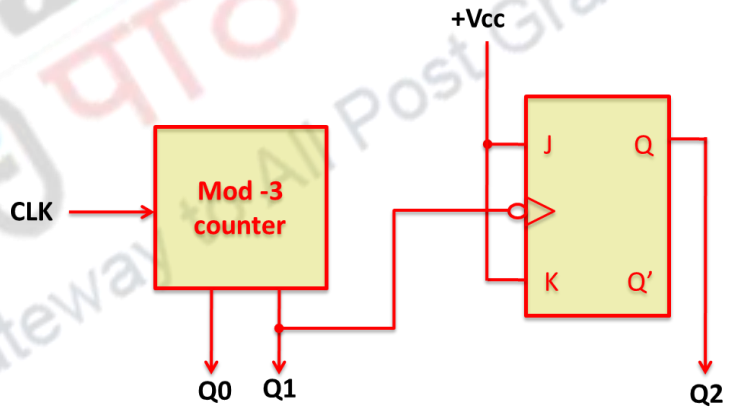


Figure 18: MOD-6 Counter

In MOD-6 counter, the counter is expected to count only 6 states. If we connect a single JK flip flop at the output of MOD-3 counter as shown in the figure 18, then the result is a 3X2 connection i.e. MOD-6 counter. The output of MOD-3 counter are labeled as Q0Q1 and output of the last FF i.e. MOD-2 counter is labeled as Q2.

IF we extend the analogy to 3x2x2 connection or 6x2 connection or 2x3x2 connection then the resulting counter is a MOD-12 counter.

8.4 MOD-10 (Decade) counter

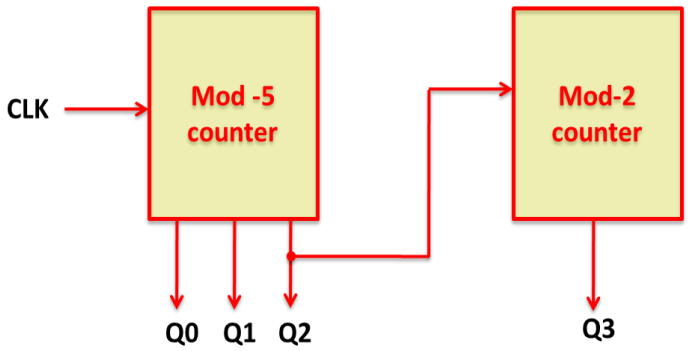


Figure 19: MOD-10 Counter

A decade or MOD-10 counter cab be constructed using the MOD-5 counter and by a JK flip flop i.e. MOD-2 counter as shown in figure 19. This counter can be obtained either by 5x2 or 2x5 connections.

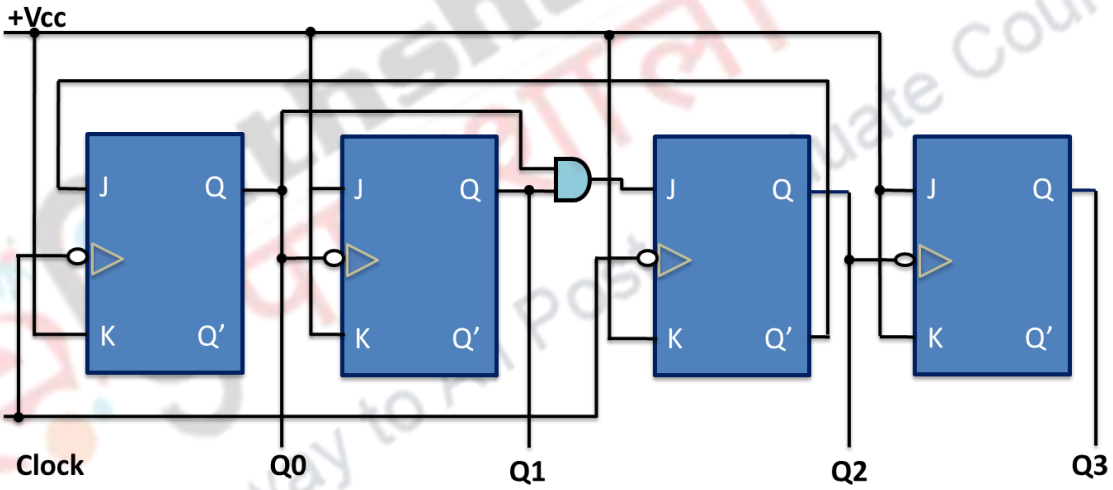


Figure 20: Decade counter

The decade counter is connected in a MOD-5 x MOD-2 connection. The clock input is applied to Mod-5 counter, the Q2 of MOD-5 is used as clock for MOD-2 counter. MOD-5 counter consist of three FFs configured in a fashion such that it counts only 5 states. After 5 states it will reset and also triggers the last FF used in MOD-2 connection as shown in figure 20. This FF toggles only after next 5 clock pulses and also resets the whole counter. The output at Q3 is symmetric but does not count the natural binary sequence. The output sequence for Q3Q2Q1Q0 is given as 0000, 0001, 0010, 0011, 0100, 1000, 1001, 1010, 1011, 1100 and resets back to 0000. This sequence is called bi-quinary sequence. The counter still counts 10 states hence it is a special MOD-10 or decade counter.

If we construct decade counter as Mod-2 x MOD-5 connection then it counts a natural binary sequence i.e. 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001 and resets back to 0000. Both configurations are valid for decade counter.

9. Counter ICs

Let us now talk about commercially available Counter ICs. In TTL family, we have range of 4 bit counters either asynchronous or synchronous configured as decade or binary counter like IC 7490, 7492, 7493 etc.. There are few ICs with up/down counting facility are available like IC 74192/193. These ICs have external clear facility for clearing the counter as shown in figure 21.

IC-TTL	Details
7490	Decade counter (separate divide by 2 and 5 sections)
7492	Divide by 12 counter (separate divide by 2 and 6 sections)
7493	4-bit binary asynchronous counter (separate 2x8)
74160	synchronous presettable 4-bit decade counter, asynchronous clear
74161	synchronous presettable 4-bit binary counter, asynchronous clear
74162	synchronous presettable 4-bit decade counter, synchronous clear
74163	synchronous presettable 4-bit binary counter, synchronous clear
74192	synchronous presettable up/down decade counter, clear
74193	synchronous presettable up/down 4-bit binary counter, clear

Figure 21: Table showing the list of TTL counter ICs

IC-CMOS	Details
4017	Decade counter (1of 10)
4020	14-bit ripple counter
4026	Decade counter with 7-segment display driver
4027	7-bit ripple counter
4029	Up/down synchronous binary/decade counter
4040	12-bir ripple counter
4060	14-bit ripple counter with internal oscillator

Figure 22: Table showing the list of CMOS counter ICs

There are several CMOS counters under CD 4000 series. IC 4017 is a decade counter, IC 4020 is a 14-bit ripple counter. In IC 4026, decade counter with 7-segment display driver is present. 4027 is a 7bit ripple counter and 4029 is a up/down synchronous binary/decade counter as shown in figure 22. Bigger 12-bit and 14 bit counters are provided by IC 4040 and 4060 respectively.

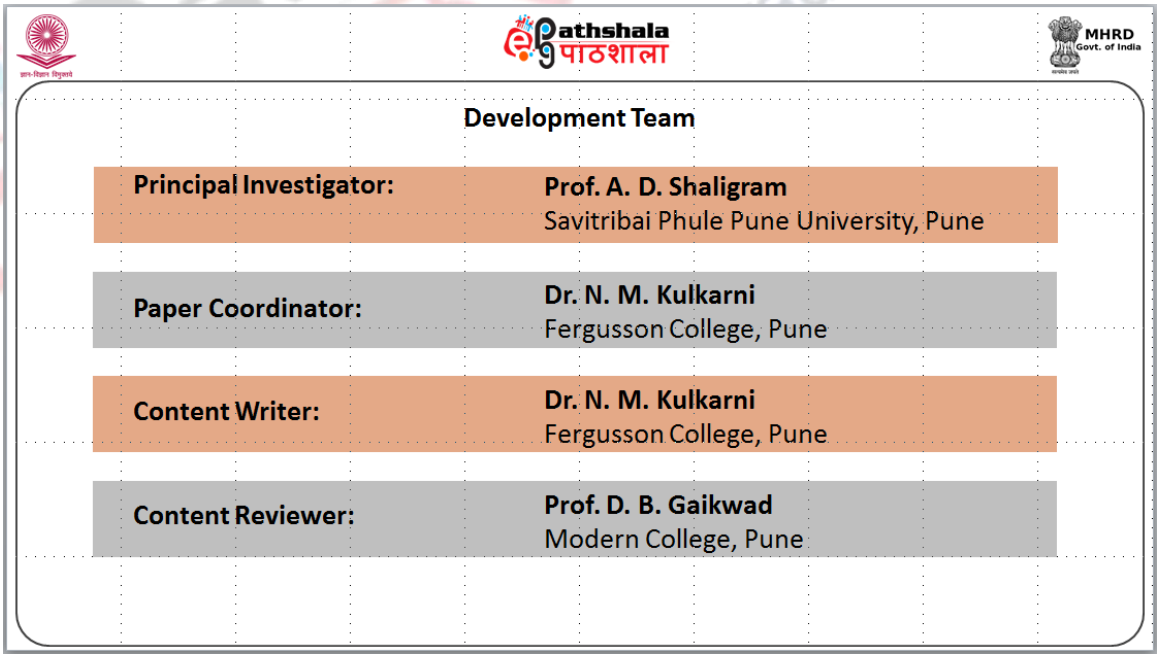
10. Applications of Counters

The digital counter is a very important and popular device that has many applications. Let us now identify the applications of the counter.

1. A digital clock
2. Auto parking system
3. Electronic Musical instruments
4. Frequency divider
5. Timer and counter
6. Parallel to serial converter
7. Resettable timer/counters
8. Traffic light controller
9. Computer keyboard

11. Summary

- Counters are used extensively for counting timing and sequencing functions.
- Asynchronous or ripple counters, in which the clock for one stage is generated from the output of the previous stage
- Synchronous counters, in which all stages are clocked simultaneously so that all the outputs change at the same time.
- Counters can count up or down.
- Modulo-*N* counters can also be produced.
- Standard integrated circuit building blocks are available to simplify the construction of counters. These can normally be cascaded to form units of any desired length.



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